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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,609	03/18/2004	Mark H. Eskridge	H0005288	9561

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EXAMINER	
NGUYEN, DILINH P	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/804,609	ESKRIDGE, MARK H.	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,10-15 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,10-15 and 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/20/04,7/29/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-5, 10-15 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (fig. 4) in view of Sugaya et al. (U.S. Pat. 6784530).

AAPA (fig. 4) disclose a micro-electromechanical system (MEMS) device, comprising:

a pair of spaced apart top and bottom substrates 14 and 20 having mutually opposing inner surfaces;

a micro-machined electromechanical device mechanism 16 coupled to the inner surface of one of the top and bottom substrates;

a metal chip bond pad 24 formed on the inner surface of the bottom substrate and being electrically coupled to an electrical path 24 (fig. 4).

AAPA (fig. 4) does not disclose a metal chip bond pad formed on the inner surface of the top substrate and a gold stud bump between the chip bond pads on the top and bottom substrates.

However, Sugaya et al. disclose a semiconductor device package comprising:

a metal chip bond pad formed on the inner surface of the top substrate 1002 in a complementary position opposite the chip bond pad 1005 on the bottom substrate;

a stud bump 1008, wherein the stud bumps are obviously formed by gold (column 7, lines 43-48), mechanically and electrically coupled between the chip bond pads on the top and bottom substrates (fig. 12B). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of AAPA by having a metal chip bond pad formed on the inner surface of the top substrate and a gold stud bump between the chip bond pads on the top and bottom substrates, as taught by Sugaya et al., in order to provide an electrical path between the top and bottom surfaces of the substrates (fig. 12B).

- Regarding claims 4 and 20, Sugaya et al. disclose that an electrical path formed on the inner surface of the top substrate 1002 and being electrically coupled to the chip bond pad (fig. 12B).
- Regarding claim 5, Sugaya et al. disclose that the electrical path formed on the inner surface of the top substrate 1002 is further electrically coupled to an upper surface of the device mechanism (fig. 12B).
- Regarding claim 10, AAPA (fig. 4) disclose a micro-electromechanical system (MEMS) device, comprising:

first and second spaced apart substrates 14 and 20 having first and second mutually opposing inner surfaces 12 and 32;

a semiconductor silicon mechanism substrate mechanically coupled to one of the inner surfaces and having a micro-electromechanical device mechanism 16 patterned therein;

a metal chip bond pad 24 formed on the inner surface of the bottom substrate and being electrically coupled to an electrical path 24 (fig. 4).

AAPA (fig. 4) does not disclose a plurality of metal chip bond pads formed on the inner surfaces of the top and bottom substrates and a gold stud bump between the chip bond pads on the top and bottom substrates.

However, Sugaya et al. disclose a semiconductor device package comprising:

a plurality of pairs of complementary chip bond pads 1005 and 1009 formed on the first and second mutually opposing inner substrate surfaces 1002 and 1007;

a stud bump 1008, wherein the stud bumps are obviously formed by gold (column 7, lines 43-48), mechanically and electrically coupled between the chip bond pads on the top and bottom substrates (fig. 12B). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of AAPA by having a plurality of metal chip bond pads formed on the inner surfaces of the top, bottom substrates and a gold stud bump between the chip bond pads on the top and bottom substrates, as taught by Sugaya et al., in order to provide an electrical path between the top and bottom surfaces of the substrates (fig. 12B).

- Regarding claim 11, Sugaya et al. disclose that a first electrical conductor formed on the first of the mutually opposing inner substrate surfaces and being electrically coupled to a first one of the chip bond pads of one of the pairs of complementary chip bond pads;

and a second electrical conductor formed on the second of the mutually oppsing inner substrate surfaces and being electrically coupled to a second one of the pair of complementary chip bond pads (fig. 12B).

- Regarding claim 12, Sugaya et al. disclose that each of the first and second electrical conductors further comprises an electrical contact 1004 being electrically coupled to the device mechanism (fig. 12B).
- Regarding claim 13, Sugaya et al. disclose that one of the first and second electrical conductors further comprises a conventional wire bond pad formed on the corresponding inner substrate surface at a position remote from the device mechanism (fig. 12B).
- Regarding claim 14, Sugaya et al. disclose that a different one of the first and second electrical conductors further comprises an electrical contact 1004 being electrically coupled to the device mechanism (fig. 12B).
- Regarding claim 15, Sugaya et al. disclose that an electrode 1004 formed on one of the first and second mutually opposing inner substrate surfaces opposite from a portion of the device mechanism and being electrically coupled to a corresponding one of the first and second electrical conductors (fig. 12B).
- Regarding claim 19, AAPA (fig. 4) disclose a micro-electromechanical system (MEMS) device, comprising:

a pair of mutually spaced apart first and second substrates 14 and 20 having mutually opposing inner surfaces;

a semiconductor silicon mechanism substrate 16 mechanically coupled to one of the inner surfaces and having a micro-machined capacitive acceleration sensor mechanism patterned therein;

an electrode 38 formed on the inner surface of the substrate;

a metal chip bond pad 24 formed on the inner surface of the bottom substrate and being electrically coupled to an electrical path 24;

one or more mesas spacing the electrodes on the first and second mutually opposing inner substrate surfaces substantially symmetrically from respective first and second surfaces of the capacitive acceleration sensor mechanism (fig. 4).

AAPA (fig. 4) does not disclose a plurality of metal chip bond pads formed on the inner surfaces of the top and bottom substrates and a gold stud bump between the chip bond pads on the top and bottom substrates.

However, Sugaya et al. disclose a semiconductor device comprising:

one or more pairs of complementary metal chip bond pads formed on the first and second mutually opposing inner substrate surfaces;

an electrical conductive path formed between one of the electrodes 1004 and one of the chip bond pads on a corresponding one of the first and second mutually opposing inner substrate surfaces; and

a stud bump 1008, wherein the stud bumps are obviously formed by gold (column 7, lines 43-48), mechanically and electrically coupled between the chip bond pads on the top and bottom substrates (fig. 12B). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to

modify the device structure of AAPA by having a plurality of metal chip bond pads formed on the inner surfaces of the top, bottom substrates and a gold stud bump between the chip bond pads on the top and bottom substrates, as taught by Sugaya et al., in order to provide an electrical path between the top and bottom surfaces of the substrates (fig. 12B).

- Regarding claim 21, Sugaya et al. disclose that a plurality of wire bond pads formed on one of the first and second mutually opposing inner substrate surfaces and an electrically conductive path formed between one of the chip bond pads and one of the wire bond pads (fig. 12B).
- Regarding claim 22, AAPA discloses that the semiconductor silicon mechanism substrate having the micro-machined capacitive acceleration sensor mechanism patterned therein is mechanically coupled to the inner surface of the first substrate; one or more mesas entend from the inner surface of the first substrate 20 and wire bond pads 26 or 24 are formed on the inner surface of the second substrate in an area remote from the sensor mechanism (fig. 4).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN

HOAI PHAM
PRIMARY EXAMINER